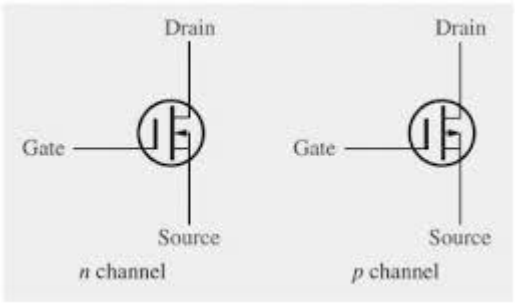
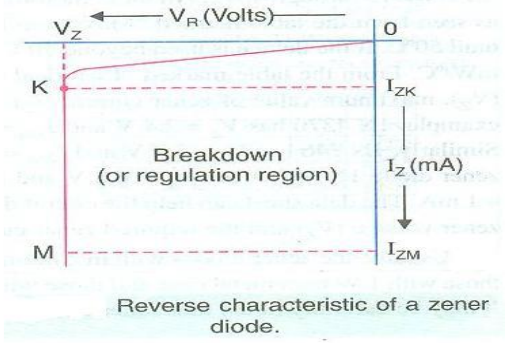
SUMMER– 18 EXAMINATION

Subject Name: Basic Electronics **Model Answer** Subject Code: 22216

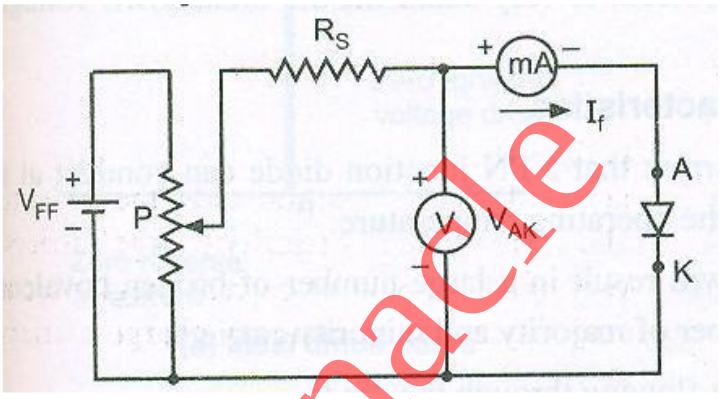
Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

<table>
<tr><th>Q. No.</th><th>Sub Q. N.</th><th>Answers</th><th>Marking Scheme</th></tr>
<tr><td>1</td><td></td><td>Attempt any FIVE:</td><td>10- Total Marks</td></tr>
<tr><td></td><td>a</td><td>State materials used for LED's to emit different colour light.</td><td>2M</td></tr>
<tr><td></td><td>Ans:</td><td>
<table>
<tr><th>Sr. No.</th><th>Material used</th><th>Colour of the emitted light</th></tr>
<tr><td>1</td><td>Gallium arsenide (GaAs)</td><td>Infrared (IR)</td></tr>
<tr><td>2</td><td>Gallium arsenide phospide GaAsP</td><td>Red or Yellow</td></tr>
<tr><td>3</td><td>Gallium phospide (GaP)</td><td>Red or Green</td></tr>
<tr><td>4</td><td>Gallium nitrite $Ga(NO_2)_3$</td><td>Blue</td></tr>
</table>
</td><td>½ Mark for each correct answer</td></tr>
<tr><td></td><td>b</td><td>Sketch the symbol of P-channel and n-channel depletion type MOSFET.</td><td>2M</td></tr>
</table>

	Ans:		**1M each**
	c	**List any two BJT biasing circuits with respect to operating point.**	**2M**
	Ans:	1) Fixed bias 2) Base biased with emitter feedback 3) Collector to base bias 4) Voltage divider bias	**Any two 1M each**
	d	**State different methods of biasing of FET.**	**2M**
	Ans:	1) Fixed bias 2) Self bias 3) Voltage divider bias 4) Source bias	**½ M each**
	e	**Sketch reverse characteristics of zener diode with proper labelling.**	**2M**
	Ans:	 Reverse characteristic of a zener diode.	**1M diagram** **1M labeling**
	f	**Define line regulation. State the formula for its regulation.**	**2M**

	Ans:	**Line regulation:-**It is the ability of the power supply to maintain its specified output voltage over changes in the input line voltage. It is expressed as percent of change in the output voltage relative to the change in the input line voltage. **Formula:-** $$Line\ regulation = \left(\frac{\Delta V_{OUT}}{\Delta V_{IN}}\right) \times 100\%$$ Δ means "a change in" **(OR)** The change in output voltage with respect to per unit change in input voltage is defined as line regulation. It is mathematically expressed as, **Line regulation=$\Delta V_L/\Delta V_S$** Where, ΔV_L = The change in output voltage ΔV_S= The change in input voltage	
	g	**State cut in voltage value of diode for silicon and germanium.**	**2M**
	Ans:	The cut in voltage value of diode for silicon is 0.7 Volt and for Germanium is 0.3 Volt	**1M each**

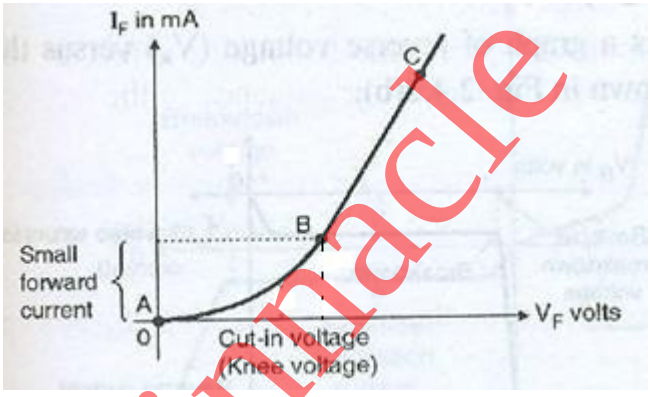
Q. No.	Sub Q. N.	Answers	Marking Scheme
2		**Attempt any THREE:**	**12- Total Marks**
	a	**Describe experimental set-up for operation of P-N junction diode in forward bias. Draw its characteristics.**	**4M**
	Ans:	**Experimental set up Forward characteristics:-** 	**2M**
		Explanation:- • PN junction diode is forward biased when positive terminal of the power supply is connected to the P-type side, and the negative terminal of the power supply is connected to the N-type side. • When a PN junction is forward biased, the holes are repelled from the positive terminal of the battery and are moved towards the junction. • Similarly the free electrons are repelled from the negative terminal of the battery and move towards the PN junction. • Because of their acquired energy (from the battery V_{FF}), some of the holes and the free electrons enter into the depletion region and recombine themselves. • This reduces the potential barrier and the width of the depleting region. • The width of depletion region and the barrier potential reduces with the increase in forward bias. • As a result of this, more majority carriers diffuse across the junction. Therefore, it	**1M**

causes a large current to flow through the PN junction. This is called forward current.

- The point at which this sudden increase in current takes place is represented as the "knee" point
- The PN junction does not permit the current to flow until the external bias voltage overcomes the barrier potential V_B. The external bias voltage should be greater than the barrier potential for the current to flow.

1M

Forward characteristics:



b	**Define alpha and beta of a transistor and state the relation between them.**	**4M**
Ans:	**Definition:** Alpha(**α)** is the current gain of CB configuration. It is defined as the ratio of collector current(I_C) to emitter current (I_E). Beta(**β)** is the current gain of CE configuration. It is defined as the ratio of collector current(I_C) to base current (I_B). **Relation between α & β:**	**1M each** **2M**

Current gain (α) of CB configuration $= \frac{I_C}{I_E}$

Current gain of (β) of CE configuration $= \frac{I_C}{I_B}$

We know that ;

$$I_E = I_B + I_C \quad \ldots\ldots(1)$$

Dividing equation (1) by I_C

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

Therefore $\frac{1}{\alpha} = \frac{1}{\beta} + 1$ [since $\alpha = \frac{I_C}{I_E}$, $\beta = \frac{I_C}{I_B}$]

Therefore $\frac{1}{\alpha} = \frac{1+\beta}{\beta}$

$\alpha(1+\beta) = \beta$

$\alpha + \alpha\beta = \beta$

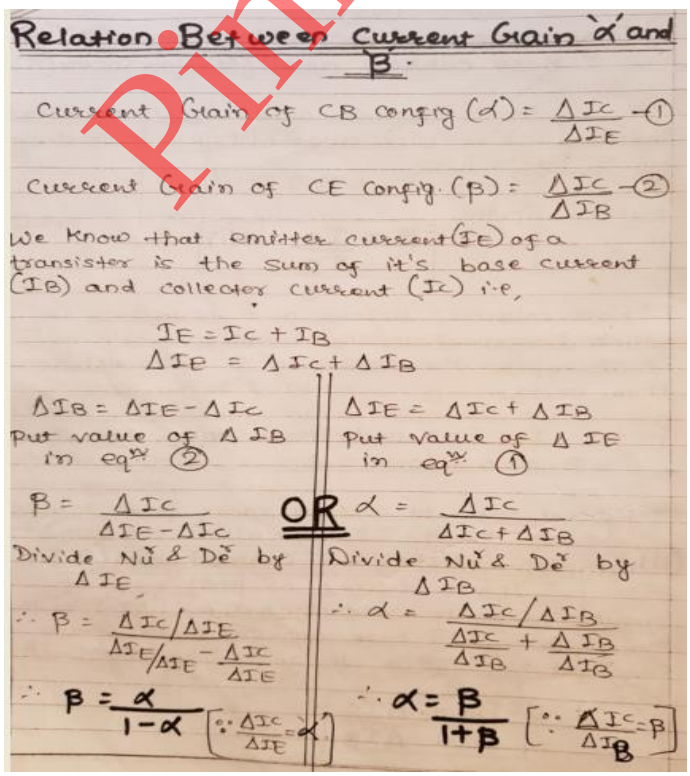
$\alpha = \beta - \alpha\beta$

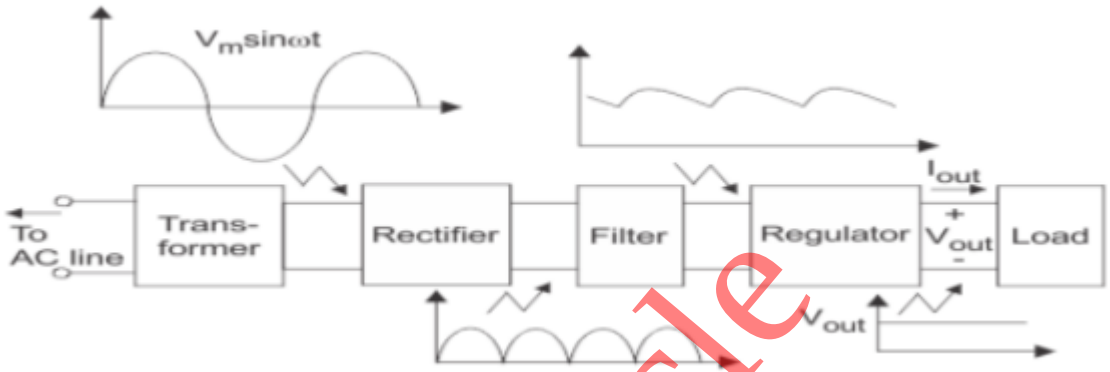
$\alpha = \beta(1-\alpha)$

Therefore $\beta = \frac{\alpha}{1-\alpha}$ $\alpha = \frac{\beta}{1+\beta}$

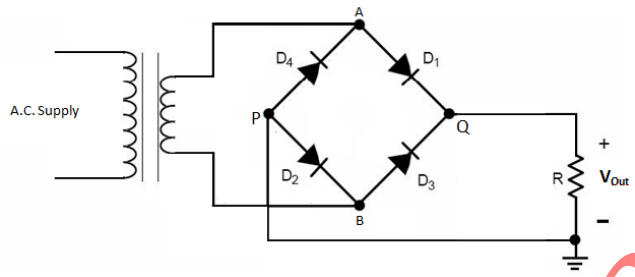
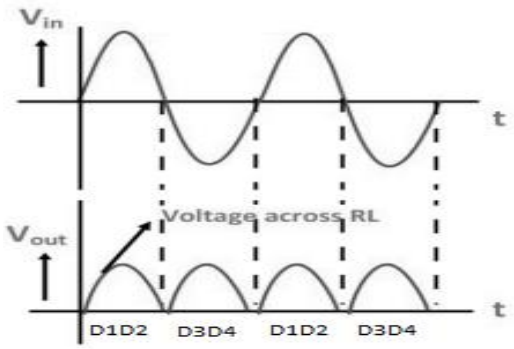
2M

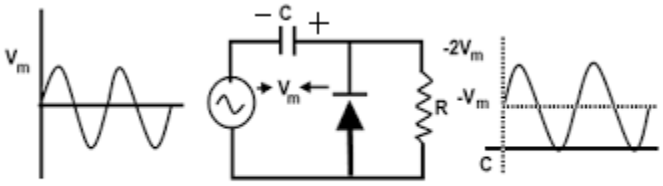
(OR)



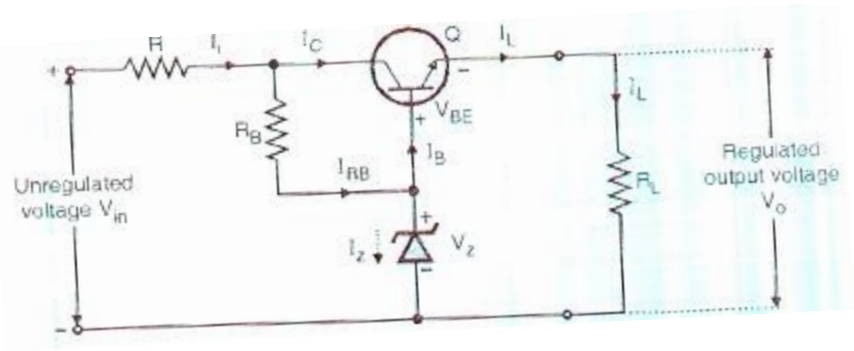
	c	**Explain basic block diagram of regulated DC power supply, draw its input and output waveforms.**	**4M**
	Ans:	**Block diagram of regulated DC power supply:-**  **Explanation** 1)Transformer 2) Rectifier 3) Filter 4) Voltage regulator. **1. Transformer:-** The AC main voltage is applied to a step down transformer. It reduces the amplitude of ac voltage to the desired level and applies it to a rectifier. **2. Rectifier:** The rectifier is usually a centre tapped or bridge type full wave rectifier. It converts the ac voltage into a pulsating dc voltage. **3. Filter:** The pulsating dc (or rectified ac) voltage contains large ripple. This voltage is applied to the filter circuit and it removes the ripple. The function of a filter is to remove the ripples to provide pure DC voltage at its output. The DC output voltage thus obtained will change with the changes in load current,input voltage, etc. So it is unregulated DC voltage. **4. Voltage Regulator :-** The unregulated DC voltage is applied to a voltage regulator. Output of the regulator circuit will be constant voltage under all operating circumstances.	**2M** **2M for explanation**

	d	**Explain the need of stabilization of Q point.**	**4M**
	Ans:	● Bias stabilization is a process of stabilizing the position of operating point "Q" ● The stabilization of Q-point is necessary to maintain the Q-point at the centre of load line because the bias point (Q-point) changes its position on the load line due to the factors such as temperature or device to device variations. ● If the Q-point gets shifted towards saturation or cut off regions, then amplified output waveform is distorted. In order to avoid such distortion it is necessary to stabilize the Q-point at the centre of the load line. ● So we need to design a biasing circuit which will keep the position of Q-point stable on the load line.	**4M**

Q. No.	Sub Q. N.	Answers	Marking Scheme
3		**Attempt any four:**	**16- Total Marks**
	a	**Describe circuit diagram of bridge rectifier, draw its input and output waveforms.**	**4M**
	Ans:	**Circuit diagram:**  When input AC signal is applied across the bridge rectifier, during the positive half cycle diodes D_1 and D_2 are forward biased and conduct while the diodes D_3 and $D_4$are reverse biased and current flows through the load from point A-D_1-load-D_2-point B. During the negative half cycle diodes D_3 and D_4 are forward biased and conduct while diodes D_1 and D_2 are reverse biased and current flow through the load from point B-D_3-load-D_4-point A. As the current flowing through the load is unidirectional, the voltage developed across the load is also unidirectional as shown in the waveform.  	**Circuit diagram2M** **Explanation 1M** **Waveform 1M**

	b	**Explain the working of positive clamper with proper circuit diagram and draw the waveforms at input & output of clamper.**	**4M**
	Ans:	**Positive clamper circuit:**  Fig. 2 Positive Clamper • The circuit will be called a positive clamper, when the signal is pushed upward by the circuit. • During the positive half cycle, the diode is reverse biased. • During the negative half cycle, it is forward biased and current flows through it. It charges the capacitor to the negative peak voltage $-V_m$ • Once the capacitor is fully charged to $-V_m$, cannot discharge because the diode cannot conduct in the reverse direction. • Therefore the capacitor acts as a battery with e.m.f equal to $-V_m$. • This voltage gets added to the input signal, $V_m . sin\,\omega t$. • Therefore the output voltage is equal to , $v_0 = V_m . \sin \omega t + V_m$ • Thus a d.c voltage equal to V_m is added to input signal. It causes the waveform to clamp positively at 0 V.	**Circuit diagram2M** **Explanation 1M** **Waveform 1M**
	c	**A JFET has I_{Dss} = 10 mA, V_P = —5 volts, gmo = 2 ms. Calculate the trans-conductance and drain current of the JFET for V_{Gs} = —2.5 volts.**	**4M**
	Ans:	The expression for drain current ID, in the saturation region is, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	**Formula-**

		$=10*10^{-3}\left(1-\frac{-2.5}{-5}\right)^2$ **=2.5mA** $g_m=\frac{I_D}{V_{GS}}$ $gm=\left\lvert\frac{2.5}{-2.5}\right\rvert$ **gm=1ʊ** **(or)** $g_m=g_{mo}\sqrt{\frac{I_D}{I_{DSS}}}$ $gm=2*\sqrt{\left(\frac{2.5}{10}\right)}$ **gm=1ʊ**	**1M each** **Correct answer-1M each**
	d	**Draw, the circuit diagram for transistor series regulator and explain functions of each component.**	**4M**

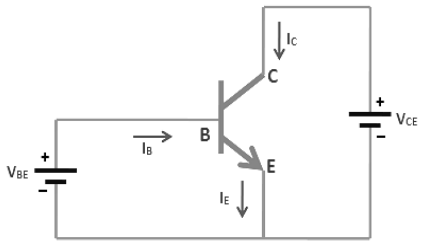
	Ans:	 Transistor (Q)- It acts as a control element and it is connected in series with the load resistor R_L. It also acts as a variable resistor to control the output voltage. Zener Diode- It provides reference voltage. Resistor (R)- It acts as a current limiting resistor. Base Resistor (R_B)-It provides biasing for transistor Q to keep the transistor in active region.	**Diagram- 2M** **Function of component- 2M**

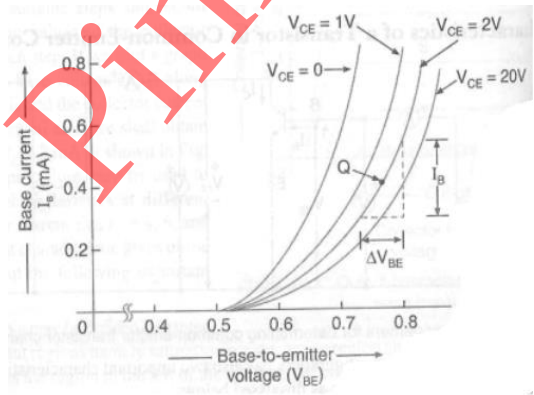
SUMMER– 18 EXAMINATION

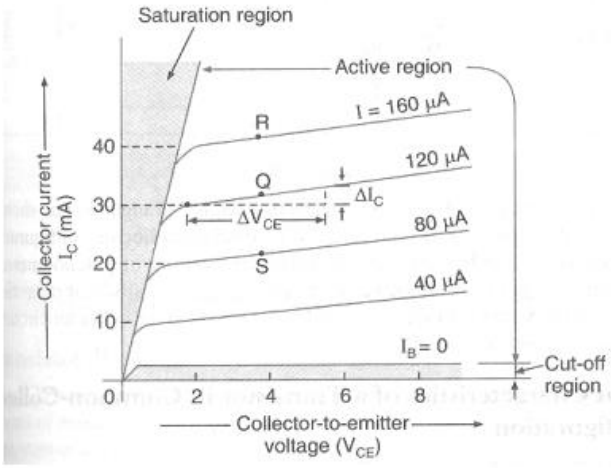
Subject Name: Basic Electronics **Model Answer** Subject Code: 22216

Q. No.	Sub Q. N.	Answers	Marking Scheme
4		**Attempt any THREE:**	12- Total Marks
	a	**State the values of following parameters for half wave and full wave rectifiers :** **(i) Number of diode used in circuit.** **(ii) Rectification efficiency (η)** **(iii) Transfer Utilization Factor (TUF)** **(iv) Ripple factor**	4M
	Ans:		1M each

Parameters	Half wave	Full wave	
		Center-tapped	Bridge
No of diodes	1	2	4
Rectification Efficiency	40.6%	81.2%	81.2%
TUF	0.287	0.693	0.812
Ripple factor	1.21	0.482	0.482

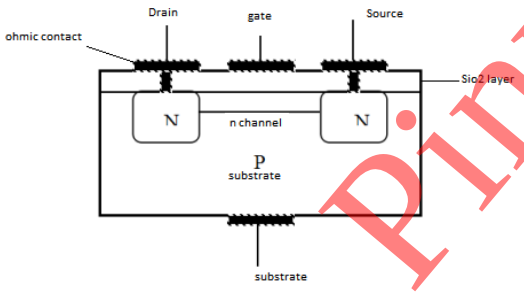
	b	**Explain the operation of NPN transistor in the active region.**	4M
	Ans:	 **Operation of NPN transistor in active region:-** Active region is one in which base emitter junction is forward biased and base collector junction will	Diagram-2M Operation-2M Note: Any other configuration can be consider

		be reverse biased in a transistor. Due to forward bias at base emitter junction, the barrier potential is reduced and results in electron flow from emitter to base or current I_E. Some of the electrons entering base region will combine with holes in the base region and result in base current I_B . Remaining large number of electrons will pass to the collector circuit and represent the collector current I_c . In the active region, the collector current increases slightly(nearly constant) as collector-emitter voltage V_{CE} increases. The value of the collector current I_C increases with the increase in I_B. In the active region $I_C = \beta I_B$.	**ed**
	c	**Draw the input and output characteristics of CE configuration with proper labelling of various regions.**	**4M**
	Ans:	 **Input characteristics of common emitter transistor**	**2M each**

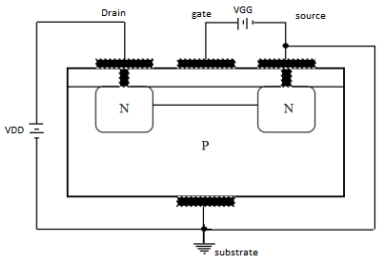


Output characteristics of common emitter transistor

d	**Draw the constructional details of n-channel MOSFET. State its working principle.**		**4M**
Ans:	Depletion type MOSFET:-		Construc tional diagram- 2M Working principle- 2M



Circuit Operation:-



The gate to source voltage is set to zero volts by the direct connection from one terminal to the other. & voltage V_{DS} is applied across the drain to source terminals. This results the attraction by the free electrons of the n channel due to positive drain & I_{DSS} establish in the circuit.

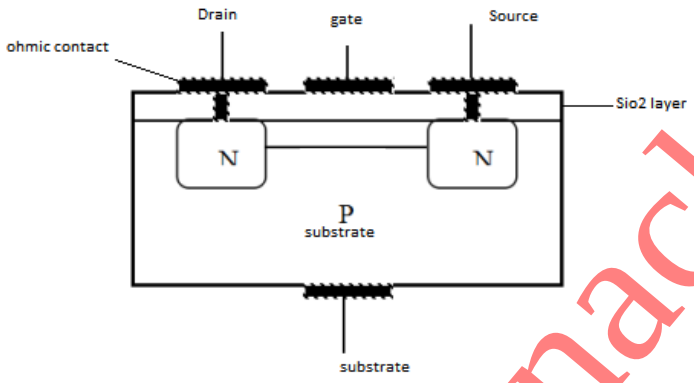
For negative voltage at gate, electrons are repelled towards P type substrate and holes are attracted towards insulated layer. Recombination occurs between electron & holes that

will reduce the number of free electrons in the channel for conduction. So drain current reduces. The value of V_{GS} at which drain current is nearly equal to zero is called cut off voltage.

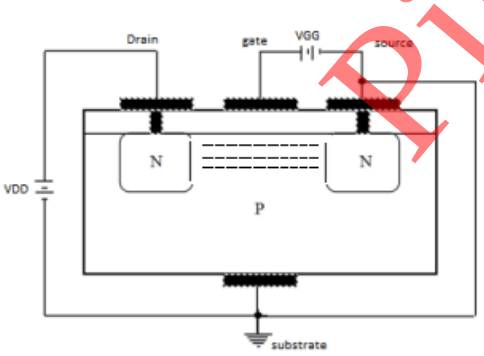
When gate is positive with respect to source, then positive V_{GS} draws additional electrons from the P type substrate. Thus drain current (I_D) increases as increase in positive V_{GS}.

OR

Enhancement – Type MOSFET:-

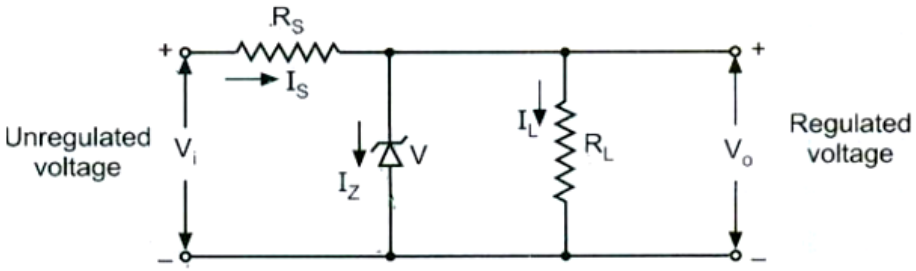


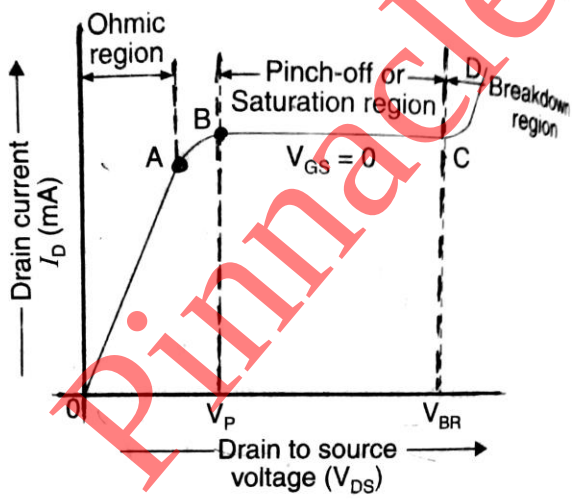
Circuit Operation:

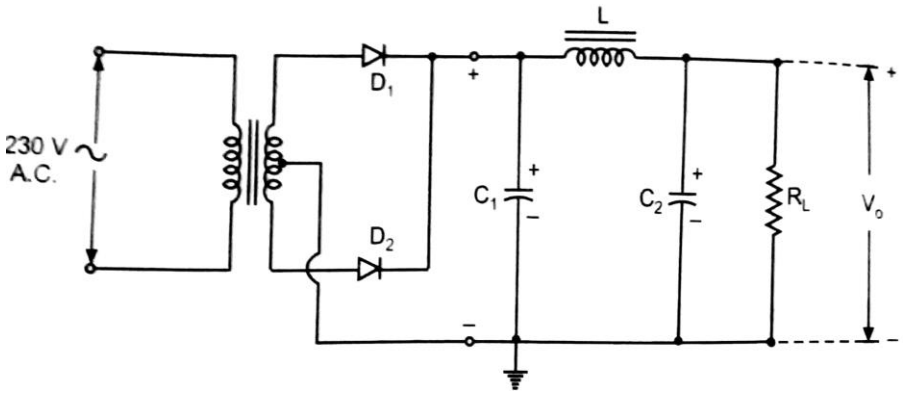


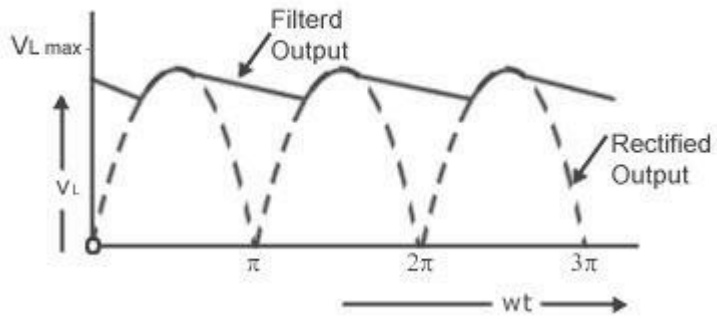
In fig. both V_{GS} & V_{DS} have been set at positive with respect to the source. The positive potential at the gate will attract the electrons from the P substrate & accumulate in the region near to the surface of SiO_2 layer. The SiO_2 layer & its insulating qualities will prevent the negative carriers (i.e. electrons) from being absorbed at the gate.

As V_{GS} increases, the concentration of electrons near the SiO_2 surface increases & there is formation of channel & the current starts following through the circuit for further applied voltage.

	e	**Describe the working of zener as a voltage regulator.**	**4M**
	Ans:	 **Zener regulator** Working For proper operation, the input voltage V_i must be greater than the Zener voltage V_z. This ensures that the Zener diode operates in the reverse breakdown condition. The unregulated input voltage V_i is applied to the Zener diode. Suppose this input voltage exceeds the Zener voltage. This voltage operates the Zener diode in reverse breakdown region and maintains a constant voltage across the load inspite of input AC voltage fluctuations or load current variations. The input current is given by, $I_S = (V_i - V_z) / R_s = (V_i - V_o) / R_s$ We know that the input current I_S is the sum of Zener current I_z and load current I_L. Therefore, $I_S = I_z + I_L$ or $I_z = I_s - I_L$ As the load current increase, the Zener current decreases so that the input current remains constant. According to Kirchhoff's voltage law, the output voltage is given by, $V_o = V_i - I_s . R_s$ As the input current is constant, the output voltage remains constant. The reverse would be true, if the load current decreases. This circuit is also correct for the changes in input voltage. As the input voltage increases, more Zener current will flow through the Zener diode. This increases the input voltage Is, and also the voltage drop across the resistor Rs, but the load voltage Vo would remain constant. The reverse would be true, if the decrease in input voltage is not below Zener voltage. Thus, a Zener diode acts as a voltage regulator and the fixed voltage is maintained across the load resistor R_L.	**Diagram 2M** **Working** **2M**

Q. No.	Sub Q. N.	Answers	Marking Scheme
5		**Attempt any TWO:**	**12- Total Marks**
	a	**Explain drain characteristics of JFET with ohmic region, saturation region, cut-off region and break down region.**	**6M**
	Ans:	 The drain characteristics of JFET can be explained as follows: Ohmic Region: This region is represented by curve OA in the figure. In this region, the drain current increases linearly with the increase in drain-to-source voltage, obeying Ohm's law. The linear increase in drain current is due to the fact that N-type semiconductor bar acts like a simple resistor. Curve AB: In this region, the drain current increases at the reverse square law rate with the increase in drain-to-source voltage. It means that drain current increases slowly as compared to that in ohmic region. It is because of the fact, that with the increase in drain-to-source voltage, the drain current increases. This in turn increases the reverse	**3 Marks for characteristics** **1 Mark for Each region**

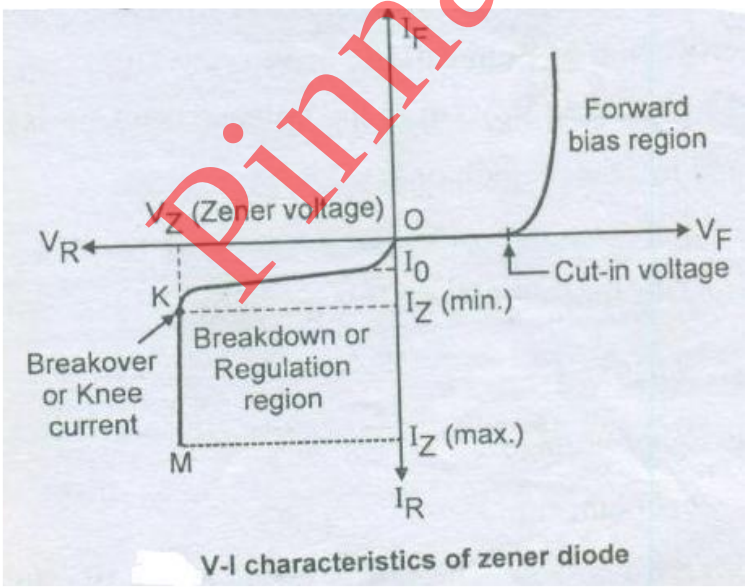
		bias voltage across the gate-source junction. As a result of this, the depletion region grows in size, thereby reducing the effective width of channel. At the drain-to-source voltage, corresponding to point B, the channel width is reduced to a minimum value and is known as pinch off. The drain-to-source voltage, at which the channel pinch-off occurs is known as pinch-off voltage (V_p) Pinch off region: This region is shown by the curve BC. It is also called saturation region or constant current region. Here the drain current remains constant at its maximum value (i.e. I_{DSS}). The drain, current in the pinch off region, depends upon the gate-to-source voltage and is given by the relation $I_D = I_{DSS}(1 - \frac{V_{GS}}{V_p})^2$ The above relation is known as Shockley's equation. The pinch off region is the normal operating region of JFET, when used as an amplifier. Breakdown region: This region is shown by the curve CD. In this region, the drain current increases rapidly as the drain-to-source voltage are increased. It happens because of the breakdown of gate-to-source junction due to avalanche effect. The drain-to-source voltage corresponding to point C is called breakdown voltage.	
b	**Draw circuit diagram and input and output waveforms of full wave rectifier connected with π filter.**	**6M**
Ans:	**Circuit diagram of full wave rectifier connected with π filter:**  **Input and Output waveforms of full wave rectifier connected with π filter**	**3Marks for Circuit diagram**



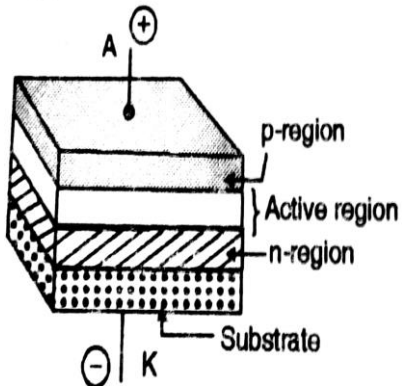
Note: In the above waveform Rectified output is Input waveform.

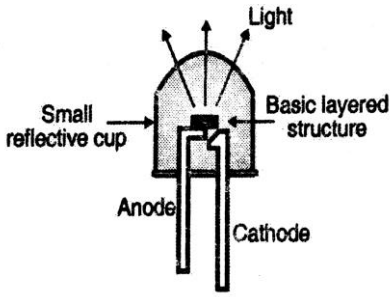
Filtered output is Output waveform.

3Marks for Input and Output waveforms

c	**Describe V-I characteristics of zener diode.**	**6M**
Ans:	 V-I characteristics of zener diode The V-I characteristics of Zener diode can be divided into two parts. 1. Forward characteristics 2. Reverse characteristics Forward characteristics : Forward characteristics of a Zener diode is similar to that of an ordinary silicon p-n junction diode.	**2 Marks for characteristics**

		It indicates that forward current is very small for voltages below knee (cut-in) voltage and large for voltages above knee voltage. Reverse characteristics : Zener diode is silicon p-n junction device which differs from a rectifier diode, in the sense, that it is operated in the reverse breakdown region. When the reverse voltage across a diode is increased a critical voltage called breakdown voltage, the reverse current increases sharply as shown in the curve KM. This is an indication that the breakdown has occurred. This breakdown voltage is called as Zener breakdown voltage or Zener voltage and it is denoted by V_Z. The breakdown voltage of Zener diode is set by carefully controlling the doping level during manufacture. After breakdown has occurred, the voltage across Zener diode remains constant equal to V_Z. Any increase in the source voltage will result in the increase in reverse Zener current.	**4 Marks for description**
Q. No.	**Sub Q. N.**	**Answers**	**Marking Scheme**
6		**Attempt any TWO:**	**12- Total Marks**
	a	**Show constructional details of LED. Give any two applications of LED.**	**6M**
	Ans:	Constructional details of LED: A pn junction diode, which emits light when forward biased, is known as a light emitting diode (LED). This emitted light may be visible or invisible. The amount of light output is directly proportional to the forward current. Thus higher the forward current, higher is the light output. Here, an N-type layer is grown on P-type substrate by a diffusion process. Then a thin P-type layer is grown on N-type layer. It has two electrodes namely Anode and Cathode. The light energy is released at the junction, when the recombination of electrons with the holes takes place. After passing through the P-region, the light is emitted through the window provided at the top of the surface.	**2 Marks for Construction**





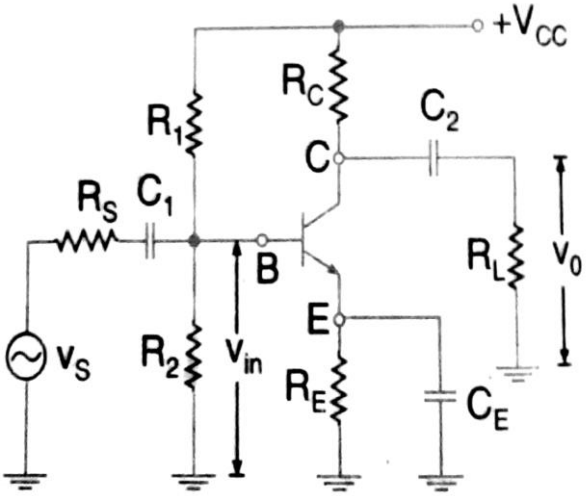
2 Marks for diagram(any one)

Applications of LED:

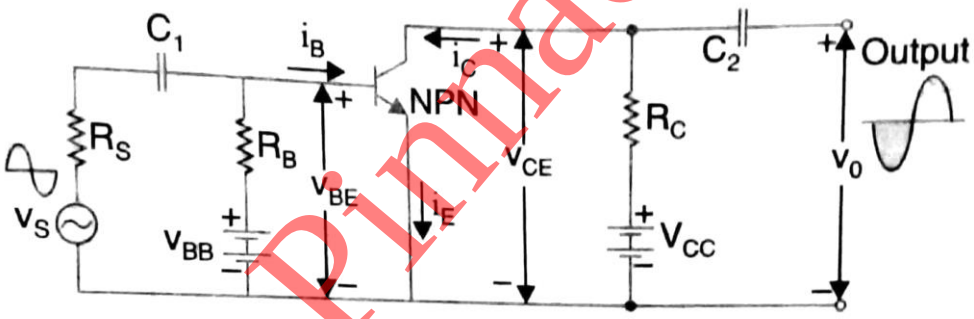
1. It is used in opto couplers.
2. It is used in optical communication systems.
3. It is used in infrared remote control.
4. It is used in 7- segment,16- segment, alphanumeric displays.
5. It is used as indicators in various electronic circuits.
6. It is used in optical switching applications.
7. It is used in burglar alarm systems.
8. It is used to indicate digital logic state.
9. Used for traffic signal management
10. Used in aviation lighting, automotive lighting, advertising and general lighting

2 Marks for any 2 Applications

b	**Describe the working of single stage CE amplifier with neat circuit diagram.**	**6M**
Ans :	**Single stage CE amplifier Circuit diagram:**	**3 Marks for any diagram**



(OR)



Working of single stage CE amplifier : — **3 Marks for working**

The circuit diagram of a voltage amplifier using single transistor in CE configuration is shown in above figure.

It is also known as a small-signal single-stage CE amplifier or RC coupled CE amplifier. It is also known as a voltage amplifier.

- The input a.c. signal is applied across the base emitter terminals of the transistor & output is taken across collector emitter terminals of the transistor.
- The potential divider biasing is provided by resistors R_1, R_2 and R_E. It provides good stabilization of the operating point.
- The capacitors C_1 and C_2 are called the coupling capacitors used to passes the AC voltage signals from one side to the other. At the same time, it does not allow the

dc voltage to pass through .Hence it is also known as blocking capacitors.

- The capacitor C_E works as a bypass capacitor. It bypasses all the AC currents from the emitter to the ground and avoids the negative current feedback. It increases the output AC voltage.
- The resistance R_L represents the resistance of whatever is connected at the output. It may be load resistance or input resistance of the next stage.

c **Differentiate clipper and clamper with following points:** **6M**

(i) Components used in circuit.

(ii) Function

(iii) Application

(iv) Configuration

Ans:

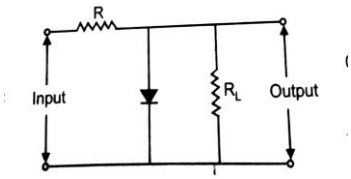
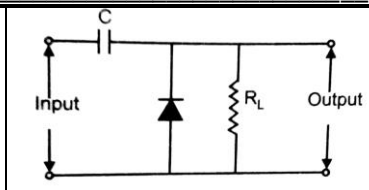
Sr.No.	Parameter	Clipper	Clamper
1	Components used in circuit	Diode, resistor	Diode, resistor, capacitor
2	Function	To remove a part of input signal voltage above or below a certain level.	To add a DC shift to the input signal
3	Application	• Digital computers, • radars, • radio and television receivers, • to limit the amplitude of the input signal voltages required in several applications.	• Used in Television receivers to restore the original dc reference signal to the video signal, • voltage multipliers.

2 Marks for Components used in circuit

1 Mark for Function

1 Mark for Application

2 Mark for Configuration

		4	Configuration			

Note: Any related configuration can be considered for clipper and clamper